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10/017,955	12/14/2001	Harry Chuang	TS01-1372	7559

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EXAMINER	
NGUYEN, TUAN H	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,955	CHUANG, HARRY	
	Examin r	Art Unit	
	Tuan H. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action responses to the RCE dated 11/07/03.

Specification

The amendment filed 11/0/03 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "the single via 11 is isolated from other close-together vias 41" as now inserted in the specification, page 12 and fig. 1a, is considered as new matter since nowhere in the original specification discloses the location of the other vias in relation to the "single via 11" as now shown in fig. 1a.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 47-77 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. This is a new matter rejection for the problem in the specification as noted above.

Claim 51 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The instant specification does not provide support for the first slot that provides stress relief at the interface of the second single via and the second copper line as now claimed. This is a new matter rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 47-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 47,

- third paragraph, "other vias formed through said first insulating layer and located elsewhere on said substrate" is indefinite since it is unclear as to where the "other vias" are located with respect to the "first single via";
- last paragraph, lines 1, 2, "said first copper line" lacks antecedent basis, does Applicant refer to the overlying copper line?

In claim 48, last paragraph, "other vias formed through said second insulating layer elsewhere on said substrate" is indefinite, it is unclear as to where the other vias are formed with respect to the second single via.

In claim 49, "said first copper line" lacks antecedent basis.

In claim 52, last line, "said interface" is confusing since it is unclear which interface is referred to (see claim 47, last paragraph for another interface).

Claims 53-69 are confusing and indefinite, it is unclear as to whether "first slot portion", "second slot portion", and "third slot portion" are portions within "a first (or second) slot" as claim in claim 47 (or 52) or they are three separated slots. How could a single slot as claimed in claim 47 (or 52) become three separated slots?

In claim 70,

- line 7, "said first single via" lacks antecedent basis;
- lines 7-9, "other vias formed through said insulating layer and located elsewhere on said substrate" is indefinite since it is unclear as to where the "other vias" are located with respect to the "single via";
- last paragraph, line 1 is confusing, it is unclear as to what is meant by "forming a slot in one or more" of the first and second copper lines, does it mean one slot is formed through first and second copper lines? line 2, "said second copper line" lacks antecedent basis, and it is unclear as to when the second copper line are formed;

Claim 71-77 are confusing and indefinite, it is unclear as to whether "first slot portion", "second slot portion", and "third slot portion" are portions within "a slot" as claim

in claim 70 or they are three separated slots. How could a single slot as claimed in claim 70 become three separated slots?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 47-77, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al (US 6,090,710) in view of Kazuhiko Kasahara (JP 3-2003321).

Andricacos et al discloses (figs 1-9, col 1-8) method for forming copper interconnects in fabrication of an integrated circuit comprising: providing a substrate having a point of electrical contact copper alloy line on substrate and having a first insulating layer (fig 8, col 6 lines 14-46); and forming a first copper interconnect to said point of electrical contact (bottom right Ist encapsulated copper alloy line on substrate, figs 8-9) through an opening in said first insulating layer (figs 9-8) wherein said first copper interconnect comprises a first single via (Cu-alloy connecting to the bottom right Ist encapsulated copper alloy line on substrate through the opening in the first insulator, fig 9) and an overlying first copper line (middle 2nd encapsulated copper alloy line on the first insulator, fig 9), said first single via being located in said opening, said overlying

first copper line overlying and being adjacent to said first insulating layer and said first single via.

Andricacos et al does not teach:

a) forming slots in said first copper line wherein said overlying first copper line being adjacent to said first single via, said slots provides stress relief at interface of said first single via and said overlying first copper line;

b) wherein said slots comprises a first slot spaced a first distance from said first single via in an X-direction, a second slot spaced a second distance from said first single via in an X-direction opposite from said X-direction of said first slot, and a third slot spaced from the first single via in Y-direction and;

c) wherein said first, second and third slots have a rectangular or square shape.

However, Kazuhiko Kasahara teaches forming slots (16, fig 2) comprising a first lot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second slot (16) spaced a second distance from said single via (15, fig 2) in an X-direction opposite from said X-direction of said first slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide wiring/metal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al by forming the first, second and third slots as in b) and c),

as taught by Kazuhiko Kasahara, to reduce stress in the overlying first copper line adjacent to the first single via for improving interconnection ability in the integrated circuit. Regarding to a), forming first, second and third slots in the overlying first copper line would provide stress relief in the interface of the first single via and the overlying first copper line in the process of Andricacos et al in view of Kazuhiko Kasahara.

With respect to claim 48, Andricacos et al (fig 9) teaches further: forming a second insulating layer overlying said first copper interconnect, and forming a second copper interconnect through said second insulating layer to said first copper interconnect wherein said second copper interconnect comprises a second single via (Cu-alloy connecting to the middle copper alloy line in the second insulator) and an overlying second copper (top 3rd encapsulated copper alloy line), said second single via being located in said second insulator, said overlying second copper line overlying and being adjacent to said second insulating layer and said second single via.

With respect to claims 51, 52, 64 and 65, Andricacos does not teach:

a') forming other slots in said overlying second copper line wherein said said slots in the overlying second copper line being adjacent to said second single via, said other slots in said overlying second copper line provide stress relief at interface between said second single via and said overlying second copper line;

b') wherein other slots comprises a first other slot spaced a first other distance from said second single via in an X-direction, a second other slot

spaced a second other distance from said second single via in an X-direction opposite from said X-direction of said first other slot, and a third other slot spaced from the second single via in Y-direction; and

c') wherein said first, second and third slots have a rectangular or square shape.

However, Kazuhiko Kasahara teaches forming slots (16, fig 2) comprising a first slot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second slot (16) spaced a second distance from the single via (15, fig 2) in an X-direction opposite from said X-direction of said srst slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide wiring/metal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al in view of Kazuhiko Kasahara for forming slots in multiple interconnect copper layer; and forming the first, second and third other slots as in b') and c'), as as taught by Kazuhiko Kasahara, to reduce stress in the copper lines adjacent to the vias for improving interconnection ability in the integrated circuit.

With respect to claims 70-72, Andricacos et al discloses (figs 1-9, col 1-8) method for forming copper interconnects in fabrication of an integrated circuit comprising:

providing a first copper line (1st right bottom encapsulated copper alloy line on

substrate, fig 8, col 6 lines 14-46) over a substrate;

forming an insulating layer (insulator, fig 8) overlying the first copper line;

forming a copper interconnect to said first copper line (bottom right lst encapsulated copper alloy line on substrate, figs 8-9) through an opening in said insulating layer (figs 9-8) wherein said copper interconnect comprises a single via (Cu-alloy connecting to the bottom right lst encapsulated copper alloy line on substrate through the opening in the first insulator, fig 9) and an overlying second copper line (middle 2nd encapsulated copper alloy line on the first insulator, fig 9), said single via being located in said opening, said second copper line overlying and being adjacent to said insulating layer and said single via.

Andricacos et al does not teach:

a") forming slots in one or more of said first and second copper lines wherein said first and second copper line being adjacent to said single via, said slots provides stress relief at interface of said first single via and one or more of said first and second copper lines; wherein said slots comprises a first slot spaced a first distance from said single via in an X-direction, a second slot spaced a second distance from

b' ') said single via in an X-direction opposite from said X-direction of said srst slot, and a third slot spaced from the single via in Y-direction; and

c") wherein said first, second and third slots have a rectangular or square shape.

However, Kazuhiko Kasahara teaches forming slots (16, 5g 2) comprising a first lot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second

slot (16) spaced a second distance from said single via (15, fig 2) in an X-direction opposite from said X-direction of said first slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide wiring/métal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al by forming the first, second and third slots as in b") and c"), as taught by Kazuhiko Kasahara, to reduce stress in one or more of the first and second copper lines for improving interconnection ability in the integrated circuit. Regarding to a"), forming slots in one or more of the first and second copper lines would provide stress relief in the interface of the single via and said one or more of said first and second copper lines in the process of Andricacos et al in view of Kazuhiko Kasahara.

With respect to claims 49, 50, 53-63, 66-69, 73-77, ranges of the overlying first copper line width, the overlying second copper line width, the first distance, the second distance, the third distance, the first slot dimension, the second slot dimension, the third slot dimension, the first other distance, the second other distance, the third other distance, the first other slot dimension, the second other slot dimension, the third other slot dimension, the overlapping distances (as shown in fig. 2 from Kasahara) are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the

selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the padicular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More padicularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See also In re Ga/fe 77 USPQ 586 (CCPA 1948),* In re Scherl 70 USPQ 204 (CCPA 194%' In re Irmscher 66 USPQ 314 (CCPA 194%. In re Norman 66 USPQ 308 (CCPA 194%,, In re Swenson 56 USPQ 372 (CCPA 1942),' In re Sola 25 USPQ 433 (CCPA 193%* In re Dreyfus 24 USPQ 52 (CCPA 1934).

Response to Arguments

Applicant's arguments filed 11/07/03 have been fully considered but they are not persuasive. Since Andricacos et al. discloses the formation of single copper via isolated from other copper vias, regardless of how far they are isolated from each others; and Kasahara teaches the formation of slots 16 in the vicinity of the single isolated via 15 and adjacent to the single isolation via 15 for relieving stress in the interconnect layer 14 (fig. 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the slots in the interconnect layer adjacent the

single isolated via as suggested by Kasahara in Andricacos et al. process for relieving stress in the interconnect metal layer and improving reliability.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 703-308-2550. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813